Customer No.: 31561
Application No.: 10/064,767
Docket No.: 8677-US-PA

REMARKS

Present Status of the Application

Applicants appreciate that the Office Action considers claims 4-5 and 14-15 to be allowable.

The Office Action rejects claims 1, 6-7, 8-11, and 16-18 under 35 U.S.C. 102 as being anticipated by Mesuda et al. (U. S. Patent 5,563,921; hereinafter Mesuda). The Office Action rejected claims 2-3 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mesuda in view of Pisipaty (U. S. Patent 6,628,112; hereinafter Pisipaty). Claims 1-18 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 102

The Office Action rejects claims 1, 6-7, 8-11, and 16-18 under 35 U.S.C. 102 as being anticipated by Mesuda. Applicants respectfully traverse the rejections for at least the reasons set forth below.

In The FINAL Action, the Office Action in "*Response to Arguments*" more specifically refers to FIG. 2 and its descriptions. However, Applicants respectfully disagree.

1. The present invention, as for example shown in FIG. 4, is to measure the jitter between the input signal S_in and the output signal S_out from the PLL. Wherein, the phase-relationship detection unit 405 can produce ***a phase relationship signal*** (jit-shrt) according to the signals S_in and S_out. In more detail (page 10, liens 8-14), the phase relation signal, output from the phase-relationship detection unit 405, is to indicate whether or not the output signal is

lead or lag.

Then, the jitter-level output unit 402 is coupled to said phase-relationship detection unit 405 and responsive to said first phase difference signal PDUP, said second phase difference signal PDDN and said phase relationship signal (jit-shrt) for generating a jitter-level output signal (jitter-out) that corresponds to the level of jitter between said output signal and said input signal of the phase locked loop.

In re Mesuda (fig. 1; fig. 2; col. 7, lines 11-17; col. 8, lines 27-39; block 17, 18) fails to disclose the features discussed above. The Office Action specifically refers to fig. 2. In fig.2, the two input signals are | fi – f3| and f2. Then considering the whole circuit as shown in fig. 1 of Mesuda, the frequency converter 14 receives the target signal with the frequency fi and the reference signal with the frequency f3. The frequency f3 is obtained by f3 = M*f2. Then, the frequency converter 14 produces the signal with frequency of | fi – f3|. The block 17 receives an output signal having the frequency |f1-f3| from the frequency converter (block 14) and an output signal having the frequency f2 from the voltage-controlled crystal oscillator (block 11), wherein f3=M * f2. The frequency f2 is feed back signal from the output of frequency converter 17 itself and several other blocks 19, 18, 20, and 11.

In Mesuda, clearly, the block 17 does not receive the input signal S_in and the output signal S_out as recited in claimed invention. The two frequency signal | fi – f3| and f2 are not the input signal S_in and the output signal S_out os the invention when considering the whole operation.

2. In the present invention, the jitter-level output unit 402 is operated with the phase-relationship detection unit 405 and responsive to said first phase difference signal PDUP, said second phase difference signal PDDN and said phase relationship signal (jit-shrt) for generating a jitter-level output signal (jitter-out) that corresponds to the level of jitter between said output signal and said input signal of the phase locked loop.

The circuit in Fig. 1 of Mesuda clearly fails to disclose the features recited in claim 1 that the jitter-level output unit 402 is coupled to the phase-relationship detection unit 405 and responsive to the first phase difference signal PDUP, the second phase difference signal PDDN and the phase relationship signal (jit-shrt) for generating a jitter-level output signal (jitter-out).

With at least the same reasons, Mesuda fails to disclose the features recited in claim 8 and 16.

3. Further still, the two phase difference signals PDUP and PDDN are generated as recited in dependent claims 6-7, 9-10, and 17-18, which are described in FIGs. 5 and 6 as the example.

With at least the foregoing reasons, claims 1, 6-7, 8-11, and 16-18 should be allowable.

Discussion of Claim Rejections under 35 USC 103

With respect to claims 2-3 and 12-13, the Office Action further cites Pisipaty in

combination. Pisipaty discloses a PLL circuit 400 in Fig. 4 (col. 5, lines 7-12). Data is fed to the D flip-flop 402 via the node 402, then a clock is output from the VCO 436. However, the PLL circuit 400 of Pisipaty does not provide the missing features in Mesuda to achieve the claimed invention. With at least the same forgoing reasons applied to claims 1 and 8, claims 2-3 and 12-13 patently define over Mesuda in view of Pisipaty.

For at least the foregoing reasons, Applicants respectfully submits that independent claims 1, 8, and 16 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-7, 9-15, and 17-18 patently define over the prior art references as well. Wherein, claims 4-5 and 14-15 are considered to be allowable.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-18 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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